Gigahertz Flexible Graphene Transistors for Microwave Integrated Circuits

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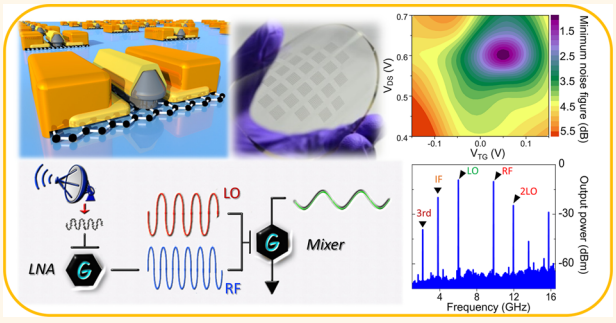
ABSTRACT Flexible integrated circuits with complex functionalities are the missing link for the active development of wearable electronic devices. Here, we report a scalable approach to fabricate self-aligned graphene microwave transistors for the implementation of flexible low-noise amplifiers and frequency mixers, two fundamental building blocks of a wireless communication receiver. A devised AlO_x T-gate structure is used to achieve an appreciable increase of device transconductance and a commensurate reduction of the associated parasitic resistance, thus yielding a remarkable extrinsic cutoff frequency of 32 GHz and a maximum oscillation frequency of 20 GHz; in both cases the operation frequency is an order of magnitude higher than previously reported. The two frequencies work at 22 and 13 GHz even when subjected to a strain of 2.5%. The gigahertz microwave integrated circuits demonstrated here pave the way for applications which require high flexibility and radio frequency operations.



KEYWORDS: graphene · radio frequency transistor · flexible electronics · low noise amplifier · frequency mixer

Flexible electronic devices built on soft materials encompass a broad range of technologies and emerging applications with significant commercial potential.[1−3] These flexible devices require uniform electrical properties over a wide range of strain conditions for applications that would not be possible using rigid electronics. This requirement presents a fundamental obstacle to the development of complex integrated circuits (ICs) such as wireless communications, which have become increasingly important for practical applications in flexible electronic devices. As such, fabrication of flexible low-noise amplifiers (LNAs) and frequency mixers, two basic ICs of a wireless receiver, plays an important role in the development of advanced portable and wearable electronics. To that end, various attempts have been pursued using conventional silicon, III−V, and even organic semiconductors.[4−7] However, despite their small size, these ICs failed to provide operation frequencies at the gigahertz level at a strain greater than 0.5%.[5,8]

Recently, Petrone *et al.* reported the development of graphene-based flexible radio frequency (RF) field-effect transistors (FETs) with both cutoff frequencies f_T and maximum oscillation frequencies f_{max} working slightly above a few gigahertz under a strain of up to 1.75%.[9] This important step was enabled by graphene's high mobility[10] and mechanical stability under strain.[11,12] Nonetheless, the reported device performance falls far short of that of an ideal graphene FET (G-FET) on a rigid substrate.[13,14] The key obstacle to further improvement is the high parasitic resistance arising from the ungated channel regions and the ultrathin metal contacts, along with the high interfacial defect density at the metal/dielectric/graphene stacks fabricated using atomic layer deposition in combination with standard e-beam lithography processes. In this paper, we report the scalable fabrication of high-performance RF G-FETs using CVD graphene as a channel material and a T-shape core−shelled Al/AlO_x as a top gate, thus enabling a significant reduction of the charged trap states at the gate/channel interface and the parasitic resistance at the source/drain contacts. The naturally formed

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aluminum oxide provides a high gating efficiency with capacitance of $C_{TG} \approx 1195$ nF/cm^2, 100 times higher than that of 300 nm-thick SiO_2. The T-shape gate structure allows for the fabrication of self-aligned source/drain contacts with increased electrode thickness, significantly reducing the access channel length and the total resistance of the transistors. The resulting flexible G-FETs exhibit field effect mobility exceeding 3000 cm^2 V^{-1} s^{-1}, with cutoff and maximum oscillation frequencies of f_T = 32 GHz and f_{max} = 20 GHz, respectively. At a strain level of 2.5%, the cutoff frequency drops to f_T = 22 GHz and the maximum oscillation frequency drops to f_{max} = 13 GHz, surpassing the performance of other reported flexible FETs. On the basis of this self-aligned device architecture, analogue RF-ICs, including LNAs and frequency mixers, are demonstrated in a gigahertz regime.

Figure 1 presents the schematic illustrations of the device process flow. Graphene used for device fabrication was grown by atmosphere-pressure CVD technique on Cu foil, followed by a wet transfer process onto a PET substrate using poly(bisphenol A carbonate) as a scaffold. A graphene strip was then defined by e-beam lithography and oxygen plasma etching. Large source/drain contacts (0.5 nm Cr/120 nm Au) were defined by e-beam lithography and thermal evaporation. To make the T-gate structure, a two-layer poly(methyl methacrylate) (PMMA) exposed twice by an e-beam writer was used to create undercuts with different widths in each layer. Following Al evaporation (450 nm), the devices were exposed to ultrahigh purity oxygen to form a thin layer of AlO_x dielectric. The van der Waals gap between Al and graphene allows oxygen molecules to penetrate deep into the interface and forming a high-quality oxide.[15] The fabrication process was completed by one additional metal evaporation of Pd (10 nm)/Au (20 nm). This deposition was automatically aligned by the Al/AlO_x gate edges and separated into two isolated regions, forming self-aligned source/drain contacts which narrowed down the noncontacted regions. This process reduced the access length (ungated region) to ~20 nm, mainly restricted to the length underneath the oxide spacer. The gate's high aspect ratio allows us to increase the thickness of the metal contacts, further lowering the device's parasitic resistance.

Figure 2 shows the optical micrograph and scanning electron microscopy images of our G-FETs on a PET substrate. The transistor features a two-finger top-gated active channel designed in a T-shape configuration. A ground-signal-ground coplanar waveguide is used to probe separate graphene RF transistors, as shown in Figure 2b. This design not only effectively extends the source/drain contact areas, but also improves the heat dissipation into the metal pads. Different gate foot lengths ranging from 0.2 to 0.8 μm were fabricated to evaluate transistor performance

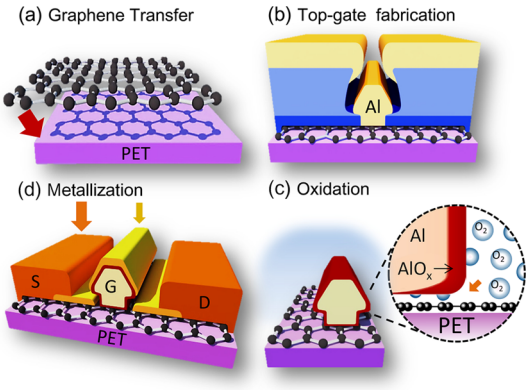

Figure 1. Schematic illustration of RF G-FET fabrication processes: (a) transfer of CVD graphene onto a PET substrate; (b) lithographical definition of aluminum T-gate using a bilayer stack of resist (PMMA as the underlayer and copolymer P(MAA-MMA) as the top layer; (c) formation of natural aluminum oxide layer using 99.999% pure oxygen for over 12 h at room temperature; (d) metalization of self-aligned source/drain contacts.

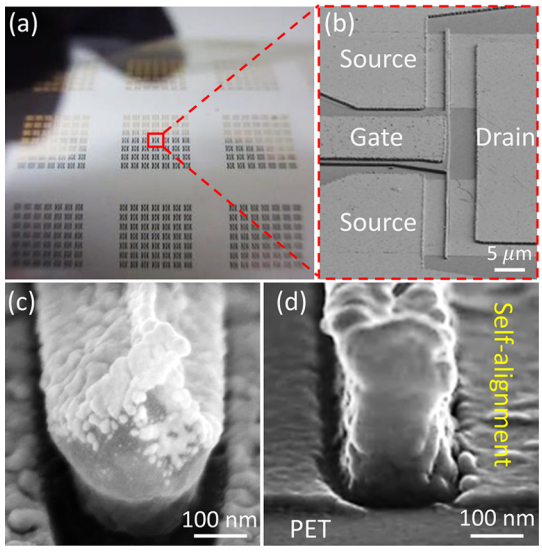

Figure 2. (a) Optical microscope image of RF G-FET array on a 4-in. bendable PET substrate. (b) SEM image of an individual device featuring the transistor structure. (c and d) Tilted SEM images of T-gate structure with difference sizes and shapes of the cap.

(Supporting Information Figure S4). Figure 2c,d shows two T-gates with different sizes of the cap. A trade-off between the resulting access channel length and the thickness of the self-aligned source/drain contacts exists. For a large cap (Figure 2c), one can increase the thickness of the self-aligned source/drain contacts while isolating the gate and source/drain contacts. However, this does not minimize access channel length. The opposite is true for gates with smaller cap sizes. Nonetheless, the thick gate structure fabricated in this study (450 nm) allows us to increase the thickness of the self-aligned source/drain contacts to 30 nm, two to three times higher than previously

reported similar structures[16−18] and effectively enhancing the maximum achievable power gain.

Figures 3 shows the room-temperature output characteristics of a typical flexible G-FET with a gate length of 200 nm under different uniaxial tensile strains in the *y*-axis direction (ε_{yy}). The inset shows the transfer characteristics at a drain voltage of 10 mV measured from $V_{TG} = -2$ to $+2$ V for each strained condition. The bending induced tensile strain is calculated through the curvature radius in a form given by $\varepsilon = t/(2r + t)$, where t is the thickness of the substrate and r is the bending radius. The charge neutrality point is found to upshift from $V_{TG} = 0$ to 0.75 V as tensile strain increases from $\varepsilon_{yy} = 0$ to 2.5%. This shift indicates a p-type doping in the graphene channel as the strain is applied. A similar but more pronounced shift has also been observed in G-FETs under strain, where the gate oxide is made of HfO_2 by atomic layer deposition.[9] That shift was attributed to the mobile trapped charges in the gate oxide and at the graphene/oxide interface.[9] In contrast to the ref 9., the naturally forming AlO_x exhibits many fewer trapped charges than HfO_2.

RESULTS AND DISCUSSION

The main panels of Figure 3 show the representative curve families ($I_{DS}-V_{DS}$) of the devices with strain increasing from ε_{yy} = 0 to 2.5%. The drain currents are plotted as a function of V_{DS} at a fixed V_{TG} in the range of 0.25 to −1.0 V with a voltage step of 0.25 V. The $I_{DS}-V_{DS}$ curves are found to be correlated to the observed shifts of the charge neutrality point. At $\varepsilon_{yy} = 0$, the drain currents start saturating at $V_{DS} > 0.3$ V. By contrast, the drain currents remain linear at the same V_{DS} as strain is applied. Note that the applied V_{DS} is restricted below 0.75 V due to the thermal constraint of the polymer substrate. High power induced Joule heating damages the substrate and the overlying graphene channel.

The main performance indexes of transistors for high-speed applications are the cutoff frequency f_T and maximum oscillation frequency f_{max}, which can be extracted from *S*-parameters. These measurements were carried out using RF probes and a network analyzer (Agilent E8361C) from 0.1 to 50 GHz, as shown in Figure 4a. To accurately evaluate the intrinsic transistor characteristics at RF frequencies, the customized test patterns on the PET substrate were designed for parasitic de-embedding, in addition to the standard open-short-load-through (SOLT) calibration procedure. The transistors are configured with grounded source contacts at both sides to ensure consistency with the coplanar RF probes. For the G-FETs with a channel length of 200 nm, a remarkable extrinsic f_T of 32 GHz and f_{max} of 20 GHz are achieved (Figure 4b,c). A careful de-embedding procedure was performed using the on-chip (flexible substrate) calibration patterns of "open" and "short" to obtain an intrinsic f_T = 64 GHz

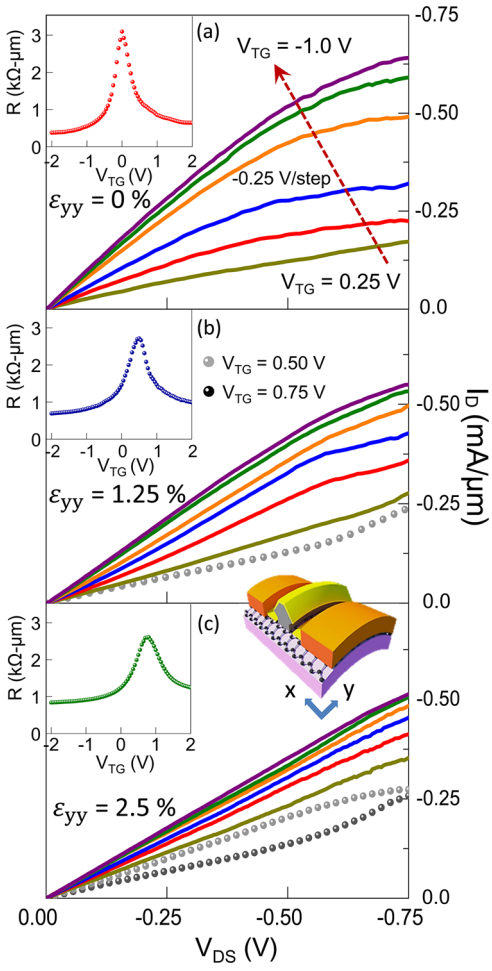

Figure 3. Transfer and output characteristics of a self-aligned G-FET on PET under different tensile strains. (a) The $I_{DS}-V_{DS}$ curves were taken at a V_{TG} from 0.25 V (bottom) to −1 V (top) in a stepwise increase of 0.25 V. Drain current saturation can be seen at a relatively lower V_{DS}. (b and c) $I_{DS}-V_{DS}$ output curves at ε_{yy} = 1.25 (b) and 2.5% (c). Dotted lines correspond to V_{TG} smaller than the voltage of charge neutrality point. Insets are the transfer $I_{DS}-V_{DS}$ curves with V_{TG} sweeping from −2 to 2 V, showing the dependence of charge neutrality point on strain.

and f_{max} = 34 GHz (Supporting Information). In our devices, the f_T is about twice as high as f_{max}, which can be attributed to the high carrier mobility and small gate length. However, the value of f_{max} is ultimately limited by the small output resistance of the G-FET on flexible substrates. It is difficult to achieve a well-behaved current saturation in G-FETs due to the inherent ambipolar transport in gapless graphene, especially for devices with a small gate length. As a result, most G-FETs present a triode-like $I_{DS}-V_{DS}$ characteristic, prohibiting strong current saturation, and the output current is linearly proportional to both the gate and drain bias voltages. The small output resistance accounts for the lower f_{max} when compared to the f_T in the same G-FETs. Following ref 19, the impact of the output resistance on f_{max} can be clearly seen from eq 1, where R_g and R_{DS} are, the gate and source-drain

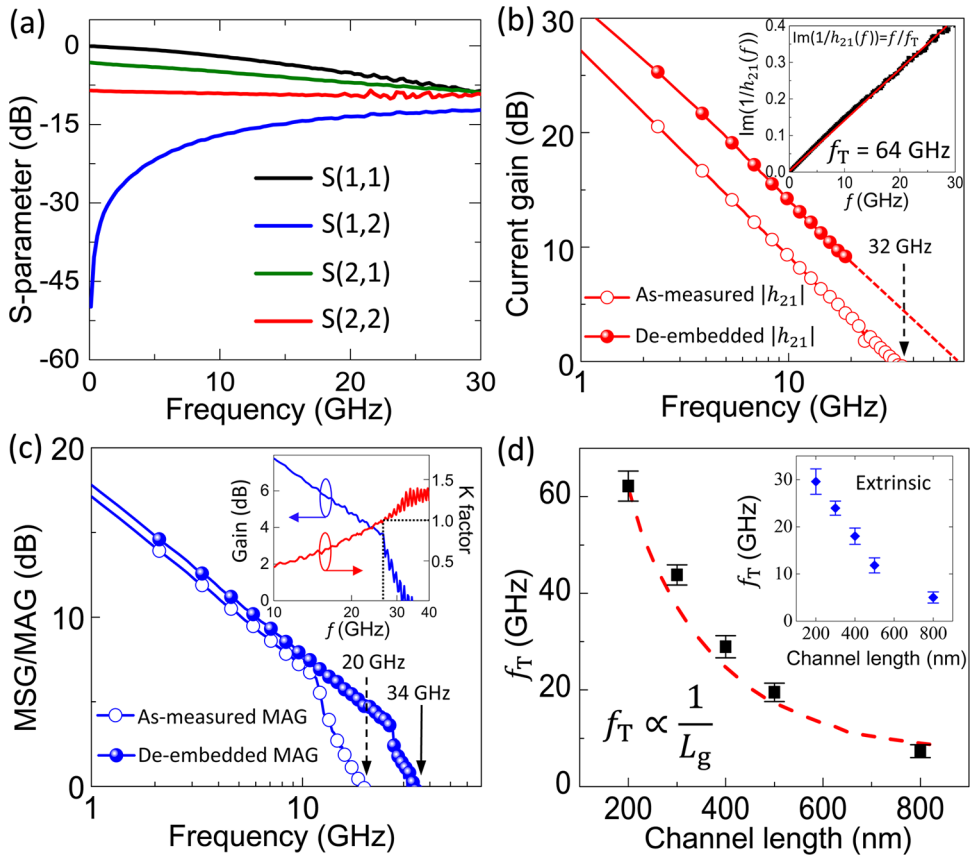

Figure 4. Radio frequency performance of G-FET with different channel lengths. (a) As-measured *S*-parameters are extracted from G-FET with 200 nm channel length. (b) Small-signal current gain $|h_{21}|$ *vs* frequency at V_{DS} = 0.7 V and L_g = 200 nm, highlighting an intrinsic and extrinsic cutoff frequency of 64 and 32 GHz, respectively. (Inset) Linear fitting using Gummel's method, showing an extraction of the cutoff frequency identical to the plot of main panel. (c) The intrinsic available power gain, MAG, shows maximum oscillation frequency exceeding 34 GHz. The inset shows the pole transition of MSG/MAG. (d) The intrinsic cutoff frequencies as a function of L_g (inset shows the extrinsic frequency).

TABLE 1. Extracted and Fitted Parameters from Small Signal RF Modeling of a G-FET with W = 80 μm and L_G = 200 nm

$\lvert g_{m,i}\rvert$	r_o	R_{gs}	R_{gd}	C_{ds}	C_{gs}	C_{gd}	L_g	L_s	L_d	R_g	R_s	R_d
52.5 mS	33 Ω	2.9 Ω	147 Ω	4.4 fF	154 fF	49.8 fF	68 pH	38.8 pH	28 pH	25 Ω	3.2 Ω	2.7Ω

parasitic resistances, respectively, C_{gd} is the gate capacitance, and $g_D = (dI_D/dV_D)$ is the output conductance.

$$f_{max} = \frac{f_T}{2\sqrt{g_D(R_g + R_{DS}) + 2\pi f_T C_{gd} R_g}} \quad (1)$$

With the small output resistance (large g_D) in G-FETs, f_{max} could be degraded significantly. We find that the extracted g_D in the G-FETs on flexible substrates (typically ~30 mS) is an order of magnitude higher than that of typical III–V semiconductor FETs.[6] The relatively large g_D plays the major role in limiting the f_{max}. On the other hand, the device cutoff frequency, which is more similar to the intrinsic property of the transistor, is inversely proportional to the gate lengths, as shown in Figure 4d. Benchmarks for other relevant competing RF technologies are summarized in Supporting Information Figure S8. The flexible G-FETs presented here demonstrate a superior f_T, outperforming the previously reported G-FETs on flexible substrates.[20−22] This is primarily due to the high transconductance achieved using naturally oxidized AlO_x which provides a high gate capacitance with low leakage current. Table 1 provides the parameters of a small-signal equivalent circuit model for a typical G-FET based on the de-embedded *S*-parameters. This work investigates the transit time (τ) analysis of a self-aligned graphene transistor with various channel lengths. This is a critical figure of merit that provides not only a physical insight into charge transport in graphene, but also valuable information for designing high-performance microwave FETs. The extracted carrier velocity in the channel is $v_h = (\partial\tau/\partial L_g)^{-1} \geq 1.2 \times 10^7$ cm/s in the linear region of the G-FET. This is much higher than the saturation velocity in Si-based devices and indicates the great potential of G-FETs applied

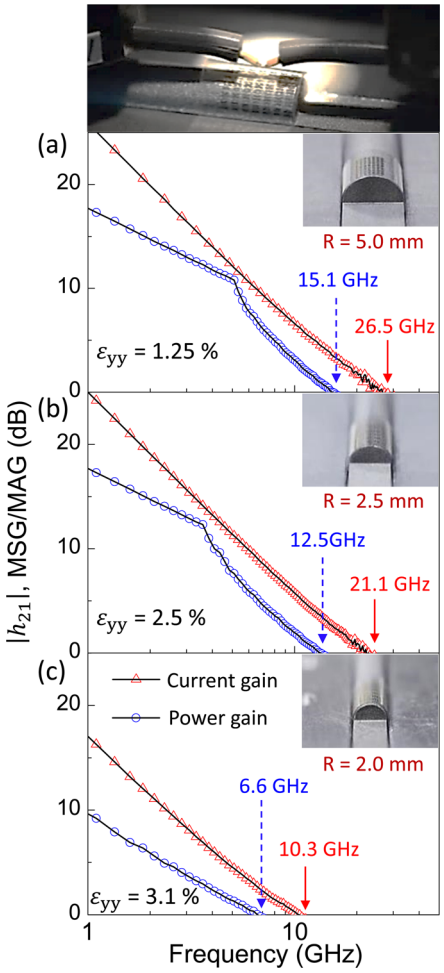

Figure 5. High-frequency device characteristics, current gain (h_{21}), and power gain (MSG/MAG), plotted as a function of frequency without being de-embedded. The tensile strain is applied through the semicylinder substrate for (a) ε_{yy} = 1.25%, (b) ε_{yy} = 2.5%, and (c) ε_{yy} = 3.1%. Insets show the optical photographs of measurement layout under different strains.

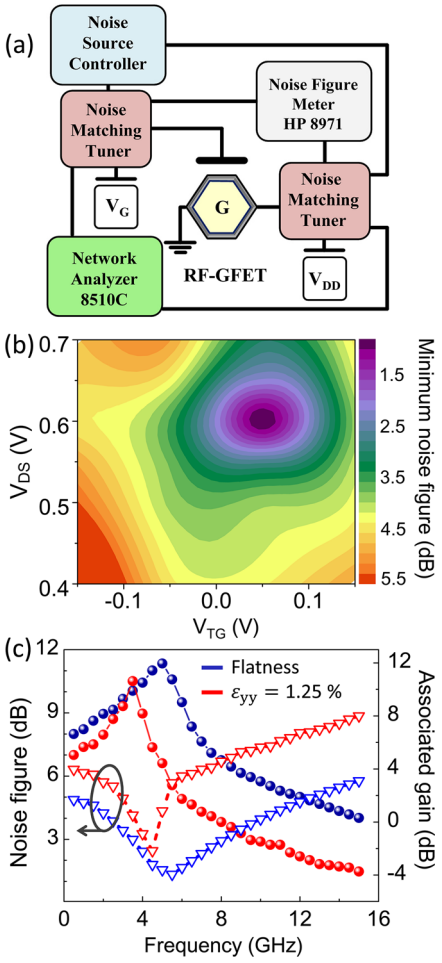

Figure 6. Characterization of low-noise amplifier (LNA). (a) Conceptual diagram of a proposed LNA measurement. (b) NF_{min} *vs* V_{TG} and V_{DS} contour plot showing suppressed noise output. (c) Peak performance at desired frequency of proposed LNA, showing the completed noise figure spectrum.

in high-speed electronics (Supporting Information Figures S10−S12).

The performance of devices on flexible substrates can be assessed by testing the mechanical reliability and stability under different strain levels. Panels a−c of Figure 5, respectively, show RF characteristics of a typical G-FET at ε_{yy} = 1.25%, ε_{yy} = 2.5%, and ε_{yy} = 3.1%. Both current and maximum available power gains are extracted from the *S*-parameters. The V_{GS} values vary with the shifted charge neutrality point at different strains to maximize device transconductance. Figure 5 shows that f_T and f_{max} degrade slightly as strain increases up to ε_{yy} = 2.5%. Further strain increase causes a significant drop in both frequencies.

The high intrinsic transconductance g_m and superior maximum oscillation frequency f_{max} enable us to further explore the possibility of using the G-FETs for realizing fully integrated circuits on flexible substrates. For example, in the front-end of a typical radio receiver, the LNA is the first active circuit in the receiver chain, and determines the sensitivity of the entire system. The transistor is tested under the setup shown in Figure 6a to emulate an LNA in actual circuits, where the tuners are set equivalent to the matching networks in a practical LNA design to evaluate the minimum noise figure (NF_{min}) and the associate gain of the G-FET. The noise figure has a critical impact on LNA characteristics, as it exhibits a strong dependence on the operating frequency in the range of V_{DS} = 0.4 to 0.7 V and V_{TG} = −0.15 to +0.15 V. In general, the g_m, f_T, and f_{max} of a G-FET strongly depend upon the gate and drain bias voltages.[16,18] It is crucial to determine the best bias point to achieve NF_{min} of the G-FET LNA. To explore the correlation between noise figure and the bias, the noise contours were measured by changing the input tuner impedance over the Smith chart. Figure 6b shows a concise 2D minimum noise figure contour plot of the graphene-based LNA at a fixed frequency of 5.5 GHz when applying different values of V_{TG} and V_{DS}. With the G-FET biased at V_{DS} = 0.6 V and V_{TG} = 0.05 V, we can obtain a decent NF_{min} of only 1.34 dB and an

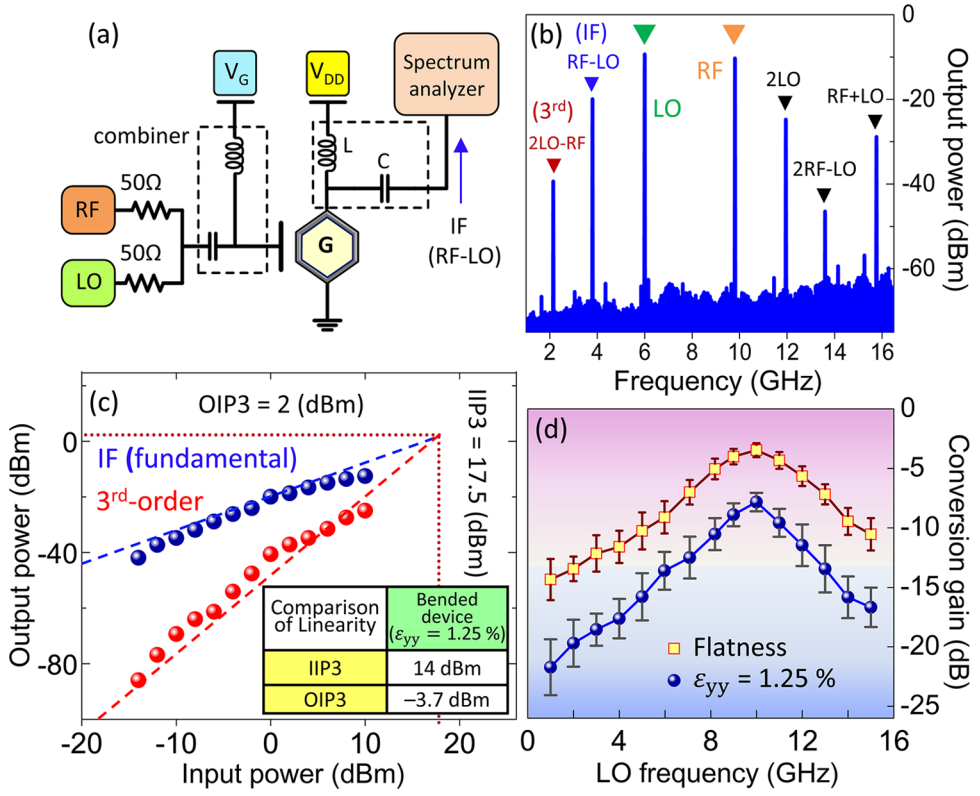

Figure 7. Frequency mixer constructed from G-FETs. (a) Schematic drawing of the circuit with two adjacent input signals: RF and LO. (b) The snapshot of output spectrum with the following parameters: LO = 5.98 GHz and RF = 9.78 GHz at equal power adjusted to 0 dBm; bias of V_{DS} = 0.7 V and V_{TG} = −0.1 V, where the linear subharmonic at 3.8 GHz (IF) clearly appears. (c) Two tone linearity test showing the output power as a function of input frequency saturation region with IP3 = 17.5 dBm. (d) Dependence of conversion gain upon different LO signals.

associated gain of 11.95 dB, suitable for use in high-performance RF front-end circuits in the gigahertz range. The graphene LNA demonstrated here is fabricated on flexible substrates, with operation frequencies in the gigahertz regime. It should be emphasized that our 200 nm graphene LNA outperforms LNAs based on III−V HEMTs,[23] and that based on typical 180 nm CMOS technology.[24,25] At the bias point and optimal impedances obtained above, the noise figure and associated gain were measured as a function of frequency, as shown in Figure 6c. The LNA presents a narrow-band characteristic with a peak gain and a minimum noise figure at the frequency around 5.5 GHz, which is consistent with the results shown in Figure 6b. For LNAs under a tensile strain (ε_{yy} = 1.25%), the noise figure slightly upshifts to ∼2.45 dB, and the operation frequency reduces to ∼4.5 GHz.

The self-aligned graphene transistor is also employed in a testing configuration to evaluate its frequency modulation capability, as shown in Figure 7a. We measured the down-conversion mixing, which is critical to demodulate the received RF signal to lower frequencies for further signal processing. First, we conducted measurements by mixing two-tone signals at 9.78 (RF signal) and 5.98 (local oscillator signal) GHz. These signals were injected into the gate electrode through a power combiner, and the output was connected to a spectrum analyzer to obtain the output signal level in the frequency domain. By manipulating the channel resistance *via* changing DC bias, the transistor served as a signal mixer owing to the nonlinear nature of device $I-V$ dependence. The as-measured response of the graphene mixers (Figure 7b) shows a relatively higher output signal intensity for the intermediate frequency ($f_{IF} = f_{RF} - f_{LO}$ = 3.8 GHz with P_{IN} = 0 dBm) tone when the device is operated at V_{TG} = −0.1 V and V_{TG} = 0.7 V (optimized g_m).[17] When V_{TG} approaches the charge neutrality point, the power spectrum shows a vanished third-order tone consistent with the ambipolar symmetry of electron and hole transport that exhibits only even-order subharmonic tones.

The frequency mixers presented here exhibit a remarkable improvement of the output power levels when compared with the reported similar devices made on rigid substrates.[17,26] In addition to the output spectra, there are two other key indexes for a frequency mixer including the 1-dB gain compression point ($P_{1\ dB}$) and the third-order intercept point (IP3), both of which allow us to further evaluate its performance. The 1-dB compression point indicates the power level at which the mixer's gain is compressed by 1 dB and the signal distortion occurs, whereas IP3 is defined by the extrapolated intersection of IF response with the two-tone third-order intermodulation (3rd-order) product composed of $2f_{RF} \pm f_{LO}$ and $2f_{LO} \pm f_{RF}$

and is an important indication for evaluating the linearity of an RF mixer. On the basis of the results shown in Supporting Information Figure S17, we obtained a $P_{1\ dB}$ of ~8 dBm at various input RF signal frequencies f_{RF} (2−10 GHz) as the RF device operated at the optimal g_m. Figure 7c shows the crucial performance index IP3 of the mixer based on the two-tone measurements. The power levels of the IF signal (f_{IF} = 3.8 GHz) and third-order intermodulation ($2f_{LO} - f_{RF}$ = 2.18 GHz) are plotted as a function of input power. Slopes of 10.5 and 28.8 dB/decade were obtained, in close agreement with the theoretical values of 10 and 30 dB/decade that are depicted as dash line in Figure 7c. The input power level of third-order intermodulation intercept (IIP3) reaches 17.5 dBm, indicating that the performance of our flexible graphene frequency mixer is comparable to those made on rigid substrates[27] and typical 180 nm CMOS technologies.[28−30]

The fabricated graphene-based frequency mixers achieved a −9.6 dB conversion gain at f_{IF} = 3.8 GHz (at f_{LO} = 5.98 GHz). In comparison, a commercially available GaAs-based passive mixer achieves a conversion gain of −7 dB at f_{IF} = 1.95 GHz.[31] Finally, the conversion gain as a function of local oscillation frequency (f_{LO}) is investigated with a fixed f_{RF} = 9.78 GHz. Figure 7d shows the performance under strain. Even applying a large bend to the device, the maximum degradation of the mixer remains within 30%.

CONCLUSION

In conclusion, the naturally self-oxidized AlO_x gate dielectric provides a high-quality metal/oxide interface and a means of fabricating scalable high-performance RF devices on soft substrates, with performance degradation of only ~30% at a tensile strain as high as 2.5%. The T-gate structure enables a self-aligned fabrication of source/drain contacts, significantly minimizing the access regions. This work is the first example of how graphene can be used for future applications of wireless communications in flexible electronics.

METHODS

Highly-Controlled Chemical Vapor Deposition of Large-Scale Graphene. Electronic-grade CVD graphene has been synthesized as competing alternative against exfoliated graphene and has been analyzed by optical and electrical measurements (see Supporting Information Figures S1 and S2).

Transistor Fabrication. A top-gated device structure is implemented by choosing 125 μm thick polyethylene terephthalate (PET) as a bendable substrate with a dielectric layer applied over the gate electrode. First, a typical polymer is coated on graphene as the supporting layer for wet-transfer process in HCl/H_2O_2 etchant solution and subsequently transferred to PET substrates, as shown in Supporting Information Figure S1b. Then, a bilayer stack of different-sensitivity poly(methyl methacrylate) (PMMA) was used as e-beam lithography resist: 996k PMMA was applied as the bottom layer, and a copolymer of methyl methacrylate and methacrylic acid P(MMA-MAA) was used as the top layer. The top layer possesses higher exposure sensitivity than that of the bottom layer so as to create a T-shape undercut which allows us to deposit a 450 nm-thick aluminum metal gate. Then, the devices were encapsulated in a sealed chamber filled with high purity oxygen (>99.999%) at a pressure of 2 kg/cm^2. After an overnight exposure, Al electrodes were surrounded with a continuous ultrathin AlO_x (<5 nm), which acts as a gate dielectric. Afterward, standard e-beam lithography process was applied to define patterns for self-alignment and external source/drain electrodes. Thermal evaporation was applied for source/drain metallization with thickness of Cr/Au (0.5 nm/120 nm) and for self-alignment contacts with thickness of Pd (10 nm)/Au (20 nm).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Part I of the Supporting Information provides the details of CVD graphene characterizations and fabrication details. Parts II and III show RF characteristics of self-aligned graphene transistors, de-embedding procedure, small-signal model extractions, evolution of relevant device parameters under bending strain, and the performance of receivers. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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